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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,408	12/12/2005	Kauko O. Laakkonen	915-001.074	5474
4955 7590 04/14/2008 WARE FRESSOLA VAN DER SLUYS & ADOLPHSON, LLP BRADFORD GREEN, BUILDING 5 755 MAIN STREET, P O BOX 224 MONROE, CT 06468			EXAMINER JANKUS, ALMIS R	
			ART UNIT 2628	PAPER NUMBER
			MAIL DATE 04/14/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/560,408

Applicant(s)

LAAKKONEN, KAUKO O.

Examiner

Almis R. Jankus

Art Unit

2628

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 December 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 December 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 12/12/05, 12/27/07.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 are presented for examination.
2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1 and 3-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Valentaten et al. in view of Niimura et al.

With respect to claim 1, Valentaten et al. teach the claimed intelligent display device connection interface integrated in the display device, at figure 2 the video circuit 16; a memory bus connected to the processor in order to realize signaling between the processor and the display device connection interface, at figure 2, the bus between the processor 14 and the RAM arbiter 18; and an adapter circuit, the RAM arbiter 18 in figure 2, in order to match signals between the memory bus and the display device connection interface, with the arbiter controlling the access to the memory bus, thereby matching the timing of the signals.

While Valentaten et al. teaches most features claimed, it is noted that figure 2 does not explicitly show a display device. However, Niimura et al. teaches a similar

arrangement and shows the display at figure 5 item 9. It would have been obvious to one of ordinary skill in the art to determine the presence of a display because Valentaten et al. shows connections to the video circuit 16 and also discusses this at column 4 lines 5-7.

Claim 8 is similar to claim 1 but is drafted in method form. Claim 8 is rejected based on the rationale presented for the rejection of claim 1 for similar respective features.

Claim 12 is similar to claim 1 but is broader in scope, and is rejected under similar rationale presented for the rejection of claim 1.

Claim 3 further requires the memory bus connected to the processor to be a non-synchronized memory bus. Niimura et al. teach this at the abstract.

Claim 4 further requires the memory bus to be for realizing signaling between the processor and a memory unit, as well as between the processor and the display device connection interface. Niimura et al. teach this at figure 5.

Claim 5 further requires the adapter circuit to include means for synchronizing the signals of the memory bus in an order required by the display device. Valentaten et al. teaches this at column 4 lines 30-35.

Claim 6 further requires the adapter circuit to be provided with gates in order to match the signals between the memory bus and the connection interface. This would have been obvious to one of ordinary skill in the art because logic gates are an integral part of digital circuitry.

Claim 7 further requires the arrangement to also include an interference protection segment in order to prevent electric interference. The instant specification describes this as known.

Claim 9 further requires the memory bus connected to the processor to be arranged to function both as a bus between the processor and a memory unit, and a bus between the processor and the display device. Niimura et al. shows this at figure 5.

Claim 10 further requires the adapter circuit used for synchronizing signals between the memory bus and the display device connection interface to be compatible. This would have been obvious in order for the arrangement to function at all.

Claim 11 further requires the memory bus and the display device connection interface to be connected by glue logics together in order to achieve communication therebetween.

This is directly apparent at Valentaten et al. at figure 2.

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Claim 13 further requires the adapter circuit to be provided with gates for synchronizing the timing of the signals between the display device connection interface and the memory bus, and for combining the connection interface and the memory bus as a physical, uniform bus. This is similar to claim 6 and is rejected under similar rationale, also taking into account figure 5 of Niimura et al.

Claim 14 is similar to claim 6 and is rejected under similar rationale.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

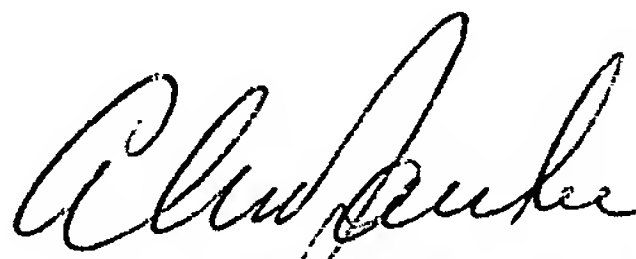
Claim 2 requires the interface to be the MeSSI by Nokia. However, this trademark adds uncertainty since it is not generally known how such an interface is defined, and furthermore, the definition of this interface could change with time.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Almis R. Jankus whose telephone number is 571-272-7643. The examiner can normally be reached on M-F, 6:30-3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 571-272-7664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AJ



ALMIS R. JANKUS
PRIMARY EXAMINER